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MIFARE Type Identification Procedure

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Document information

Info	Content
Keywords	MIFARE, ISO/IEC 14443
Abstract	This document describes how to differentiate between the members of the MIFARE card IC family. ISO/IEC 14443-3 describes the initialization and anticollision procedure, and ISO/IEC 14443-4 describes the protocol activation procedure. This document shows how to use these procedures to deliver the chip type information for all MIFARE ICs.

Revision history

Rev	Date	Description
3.1	20090707	Correction of Table 12
3	20090518	Third release (supersedes AN MIFARE Interface Platform, Type Identification Procedure, Rev. 1.3, Nov. 2004)

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1. Introduction

1.1 Terms and Abbreviations

Table 1 shows the terms and abbreviation used in this document. All the “Type A” related definitions are used and described in the ISO/IEC 14443 documents.

Table 1. Abbreviatons

Abbreviation	
ATQA	Answer To Request acc. to ISO/IEC 14443-4
ATS	Answer To Select acc. to ISO/IEC 14443-4
DIF	Dual Interface (cards)
COS	Card Operating System
CL	Cascade Level acc. to ISO/IEC 14443-3
CT	Cascade Tag, Type A
n.a.	not applicable
NFC	Near Field Communication
PCD	Proximity Coupling Device (“Contactless Reader”)
PICC	Proximity Integrated Circuit (“Contactless Card”)
PKE	Public Key Encryption (like RSA or ECC)
REQA	Request Command, Type A
SAK	Select Acknowledge, Type A
Select	Select Command, Type A
RID	Random ID, typically dynamically generated at Power-on Reset (UID0 = “0x08”, Random number in UID1… UID3)
RFU	Reserved for future use
UID	Unique Identifier, Type A

1.2 Scope

This document describes how to differentiate between the members of the MIFARE interface card IC family. The ISO/IEC 14443-3 describes the initialisation and anticollision procedure for type A, which delivers the card type information for all MIFARE cards.

The MIFARE cards are ISO/IEC 14443-3 compatible. Therefore already existing applications can easily be extended to operate with newer MIFARE chips respectively all other ISO/IEC 14443-3 compatible PICCs.

This document provides an easy guideline how the ISO/IEC 14443 compatible PCD should handle the MIFARE cards and how it can distinguish between the different available types of MIFARE cards.

1.3 MIFARE and ISO/IEC 14443

1.3.1 MIFARE

All MIFARE ICs are compliant to the ISO/IEC 14443 part 1, part 2 and part 3. The T=CL protocol as defined in the ISO/IEC 14443-4 is supported by MIFARE DESFire, the NXP Dual or Triple Interface Card ICs (like SmartMX), and the MIFARE Plus.

The MIFARE 1K, the MIFARE Mini, the MIFARE 4K, the MIFARE Ultralight, the MIFARE Ultralight C and the MIFARE Plus in the security level 1 and 2 use the MIFARE Protocol.

The MIFARE 1K, the MIFARE Mini, and the MIFARE 4K use the proprietary MIFARE Crypto 1, and are called MIFARE 1K/4K/Mini.

1.3.2 ISO/IEC 14443

The ISO/IEC 14443 consists of 4 parts.

1.3.2.1 Part 1: Physical characteristics

The ISO/IEC 14443-1 defines the physical size of the ISO/IEC 14443 PICC and its antenna.

1.3.2.2 Part 2: RF signal & power interface

The ISO/IEC 14443-2 defines the carrier frequency of 13.56 MHz, the modulation and coding, and the minimum and maximum field-strength. It is split up into type A (= MIFARE) and type B.

1.3.2.3 Part 3: Initialisation & anti-collision

The ISO/IEC 14443-3 defines the start of communication and how to select the PICC. Sometimes this is called “Card Activation Sequence”. It is split up into type A (= MIFARE) and type B.

1.3.2.4 Part 4: Transmission protocol

The ISO/IEC 14443-4 defines the protocol for a data exchange between PCD and PICC. This protocol often is called “T=CL” protocol.

Please refer to the ISO/IEC 14443 documents for details.

2. MIFARE IC types

The Table 2 shows the NXP MIFARE ICs and their features, Table 3 shows the supported ISO layers.

Table 2. NXP Contactless Card IC Feature Overview

	MIFARE Ultralight	MIFARE Ultralight C	MIFARE 1K/4K/Mini	MIFARE Plus	MIFARE DESFire	DIF (like SmartMX)
HW Crypto	-	3DES	Crypto1	Crypto1, AES	3DES, AES	3DES, AES, PKE
EEPROM	512 bit	1536 bit	320 Bytes, 1k Bytes, 4k Bytes	2k Bytes, 4k Bytes	2k Bytes, 4k Bytes, 8k Bytes	4k Bytes – 144k Bytes
Special Features	-	-	-	MIFARE 1K/4K/Mini compatible	-	MIFARE 1K/4K/Mini compatible
Certification	-	-	-	CC EAL 4+	CC EAL 4+	CC EAL 5+
Contactless interface	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A	ISO/IEC 14443A

Table 3. NXP Contactless Card IC compliance overview

ISO layer	MIFARE Ultralight	MIFARE Ultralight C	MIFARE 1K/4K/Mini	MIFARE Plus	MIFARE DESFire	SmartMX platform
ISO/IEC 14443 -4				✓[1]	✓	✓
ISO/IEC 14443 -3	✓	✓	✓	✓	✓	✓
ISO/IEC 14443 -2	✓	✓	✓	✓	✓	✓
ISO/IEC 14443 -1				✓[2]		

1. The MIFARE Plus supports the ISO /IEC 14443-4 protocol in all security levels, but only in security level 3 the SAK indicates the ISO/IEC 14443-4 compliance.
2. Depends on the card design, the IC alone cannot meet the physical characteristics.

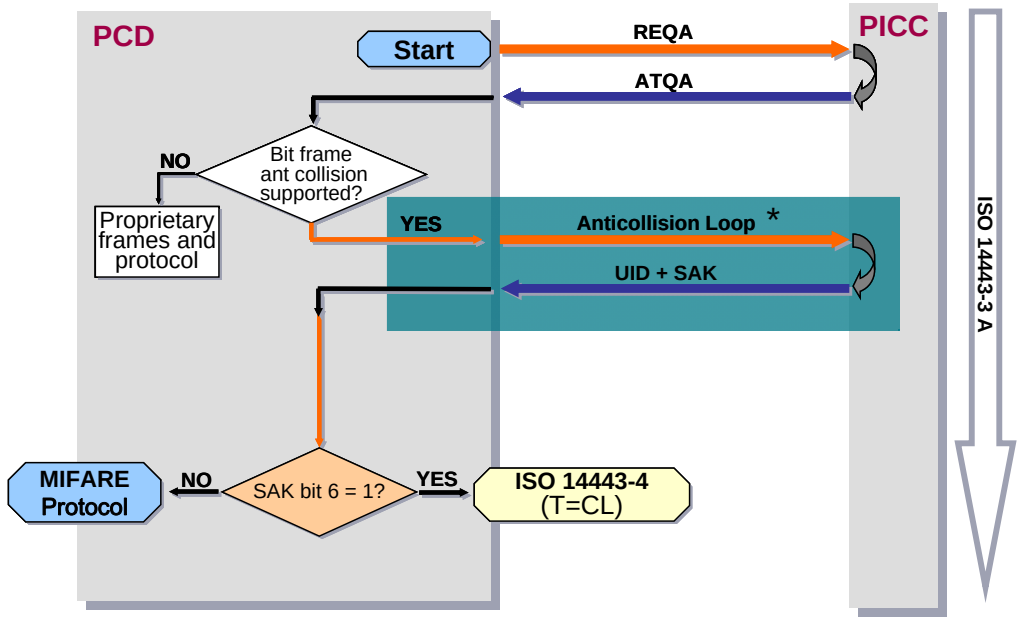
3. Chip Type Identification Procedure

The PCD typically polls for PICCs in the field. This is done with the REQA. When a PICC is within the operating range of the PCD and receives the REQA, any MIFARE PICC returns the ATQA.

The content of the ATQA should be ignored in a real application, even though according to the ISO/IEC 14443 it indicates that the PICC supports the Anticollision scheme.

Note: In the case of two or more MIFARE PICCs are in the operating field of the PCD at the same time, the received (combined) ATQA might contain “collisions”. That means there might be no unambiguous content anyway.

The complete card activation sequence is shown in the Fig 1 and Fig 2. The bit 6[3] in the SAK indicates, whether the PICC is compliant to the ISO/IEC14443-4 or not. However, it does not necessarily indicate, whether the PICC supports the MIFARE Protocol or not. For more details about selecting the different type of MIFARE cards refer to the AN “MIFARE ISO/IEC 14443 PICC Selection”.

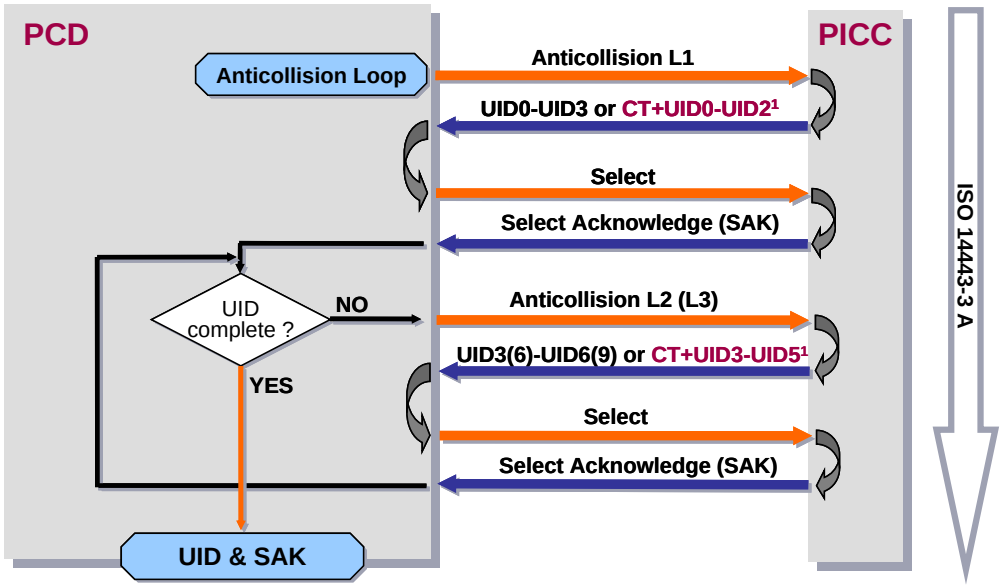


(1) Details of the Anticollision Loop see Fig 2.

Fig 1. Principle of the Card Activation Sequence

Note: For more details regarding the selection of one of the different types of MIFARE cards based on the SAK refer to AN 130830 “MIFARE ISO/IEC 14443 PICC Selection”.

3. Attention: The bit numbering in the ISO/IEC 14443 document starts with bit 1 … 8, but not bit 0…7.



(1) The CT (= Cascade Tag, Type A) byte indicates that the UID is not received completely yet. It indicates that another anticollision loop on the next higher cascade level is required to get the complete UID.

Fig 2. Anticollision Loop as part of the Card Activation Sequence

3.1 Coding of Answer to Request Type A (ATQA)

Table 4 shows the coding of the ATQA as described in the ISO/IEC 14443-3. The RFU marked bits must be set to “0”, the proprietary bits might be used for proprietary codings. In real application the content details of the ATQA are recommended to be ignored anyway.

Table 5 shows the ATQA coding of the NXP card ICs.

Note 1: The bit numbering in the ISO/IEC 14443 starts with LSBit = bit 1, but not LSBit = bit 0. So one byte counts bit 1…8 instead of bit 0…7.

Note 2: The ISO/IEC 14443 transfers LSByte first. So e.g. 0x 00 44 (ATQA of the MF UL) is often received as 0x 44 00.

Table 4. ATQA Coding according to the ISO/IEC 14443-3

Bit number	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ISO/IEC 14443-3	RFU				Proprietary				UIDsize		RFU	Bit Frame Anticollision				
Proprietary	0	0	0	0				1			0					
	0	0	0	0			1				0					
	0	0	0	0		1					0					
Single Size UID	0	0	0	0					0	0	0					
Double Size UID	0	0	0	0					0	1	0					
Triple Size UID	0	0	0	0					1	0	0					
RFU	0	0	0	0					1	1	0					
Anticollision supported	0	0	0	0							0	1	0	0	0	0
	0	0	0	0							0	0	1	0	0	0
	0	0	0	0							0	0	0	1	0	0
	0	0	0	0							0	0	0	0	1	0
	0	0	0	0							0	0	0	0	0	1

Table 5. ATQA Coding of NXP Contactless Card ICs

X: depends on the COS

Bit number	Hex Value	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ISO/IEC 14443-3		RFU				Proprietary				UID size		RFU	Bit Frame Anticollision				
MIFARE Ultralight	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE Ultralight C	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE Mini	00 04	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
MIFARE 1K	00 04	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
MIFARE 4K	00 02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
MIFARE Plus (4 Byte UID or 4 Byte RID)	00 04	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
MIFARE Plus (4 Byte UID or 4 Byte RID)	00 02	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
MIFARE Plus (7 Byte UID)	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
MIFARE Plus (7 Byte UID)	00 42	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0
MIFARE DESFire	03 44	0	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0
P3SR008	00 44	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0
SmartMX with MIFARE 1K emulation	0X 04	0	0	0	0	x	x	x	x	0	0	0	0	0	1	0	0
SmartMX with MIFARE 4K emulation	0X 02	0	0	0	0	x	x	x	x	0	0	0	0	0	0	1	0
SmartMX with 7 Byte UID	0X 48	0	0	0	0	x	x	x	x	0	1	0	0	1	0	0	0

3.2 Coding of Select Acknowledge (SAK)

Table 6 shows the coding of the SAK of the NXP card ICs as described in the ISO/IEC 14443-3. It indicates the ISO/IEC 18092 protocol compliance, too. The RFU marked bits must be set to “0”, the proprietary bits might be used for proprietary coding.

In case of double size UIDs or triple size UIDs always **only** the last SAK shall be used to distinguish the chip type.

Note: RIDs always use the size of single size UIDs (4 Bytes).

Table 6. SAK coding of NXP Contactless Card ICs

Coding according to the ISO/IEC 14443-3 and ISO/IEC 18092, X = do not care

Bit number	UID size	Memory	Sec. Level	Hex Value	8	7	6	5	4	3	2	1
UID not complete				04	0	0	0	0	0	1	0	0
UID complete, PICC compliant with ISO/IEC 14443-4					X	X	1	X	X	0	X	X
UID complete, PICC not compliant with ISO/IEC 14443-4					X	X	0	X	X	0	X	X
UID complete, PICC compliant with ISO/IEC 18092 (NFC)					X	1	X	X	X	0	X	X
UID complete, PICC not compliant with ISO/IEC 18092					X	0	X	X	X	0	X	X
Any MIFARE CL1[4]	double			04	0	0	0	0	0	1	0	0
MIFARE DESFire CL1	double	-	-	24	0	0	1	0	0	1	0	0
MIFARE DESFire EV1 CL1	double	-	-	24	0	0	1	0	0	1	0	0
MIFARE Ultralight CL2	double			00	0	0	0	0	0	0	0	0
MIFARE Ultralight C CL2	double			00	0	0	0	0	0	0	0	0
MIFARE Mini	single	0.3K	-	09	0	0	0	0	1	0	0	1
MIFARE 1K	single	1K	-	08	0	0	0	0	1	0	0	0
MIFARE 4K	single	4K	-	18	0	0	0	1	1	0	0	0
MIFARE Plus	single	2K	1	08	0	0	0	0	1	0	0	0
MIFARE Plus	single	4K	1	18	0	0	0	1	1	0	0	0
MIFARE Plus CL2	double	2K	1	08	0	0	0	0	1	0	0	0
MIFARE Plus CL2	double	4K	1	18	0	0	0	1	1	0	0	0
MIFARE Plus	single	2K	2	10	0	0	0	1	0	0	0	0
MIFARE Plus	single	4K	2	11	0	0	0	1	0	0	0	1
MIFARE Plus CL2	double	2K	2	10	0	0	0	1	0	0	0	0
MIFARE Plus CL2	double	4K	2	11	0	0	0	1	0	0	0	1
MIFARE Plus	single	2K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus	single	4K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus CL2	double	2K	3	20	0	0	1	0	0	0	0	0
MIFARE Plus CL2	double	4K	3	20	0	0	1	0	0	0	0	0
MIFARE DESFire CL2	double	4K	-	20	0	0	1	0	0	0	0	0
MIFARE DESFire EV1 CL2	double	2K	-	20	0	0	1	0	0	0	0	0
MIFARE DESFire EV1 CL2	double	4K	-	20	0	0	1	0	0	0	0	0
MIFARE DESFire EV1 CL2	double	8K	-	20	0	0	1	0	0	0	0	0

4. Except the DESFire and DESFire EV1.

Bit number	UID size	Memory	Sec. Level	Hex Value	8	7	6	5	4	3	2	1
Smart MX	single	-	-	xx[5]	x	x	x	x	x	x	x	x
Smart MX CL2	double	-	-	xx[6]	x	x	x	x	x	x	x	x

Note: The bit numbering in the ISO/IEC 14443 starts with LSBit = bit 1, but not LSBit = bit 0. So one byte counts bit 1…8 instead of bit 0…7.

Note: NXP MIFARE Plus ICs might use a **generic SAK** (in the near future), which does not (exclusively) indicate the chip type during the anticollision procedure for privacy reasons. In such case the way to distinguish between different MIFARE Plus types is the read of Block 0, to use the ATS, if available, or the card capabilities of the Virtual Card Selection.

4. Coding of Type Identification in the Historical Characters of the ATS

New MIFARE card ICs using the ISO/IEC 14443-4 may offer the option to code the ATS in the field. This allows the user to code an own chip type. The Type Identification coding as used by the MIFARE Plus is shown in Table 7.

It is not recommended to code any application related information in the publicly available data like ATS.

Note: Be aware of privacy protection and avoid as much information being available to anybody in plain as possible.

4.1 Type Identification Coding format

The format of the Type Identification Coding is shown in Table 7. It uses a TLV format (details refer to ISO/IEC 7816-4), starting with an Tag Byte.

The Tag Byte is followed by a Length byte, indicating the length of the following Value field. The value bytes code the Chip Type, the Chip Version, the Specifics and a 2 byte CRC. The Length byte counts the number of value bytes including the CRC, but excluding the length byte itself.

The CRC for the Type Identification Coding is calculated as described in the ISO/IEC 14443 type A, and ensures a proper reading of the Type Identification Coding.

Table 7. Type Identification Coding in the Historical Characters

	Tag	Length	Chip Type	Chip Version	Specifics	CRC
no. of bytes	1	1	1	1	1	2
Content	see 4.2	05_{hex}	see 4.3	see 4.4	see 4.5	CRC
Example (hex)	C1	05	2F	2F	01	BC D6

5. Depends on the COS.
6. Depends on the COS.

4.2 Tag Byte

The Tag Byte indicates the presence of a Historical Character pattern using a TLV format (see Table 8). The Value $C1_{hex}$ is coded as private class and primitive object (ISO/IEC 7816-4), and is used as default value for MIFARE or virtual cards of various types.

Table 8. Tag Byte

	b7	b6	b6	b5	b4	b3	b2	b1	b0	Hex
MIFARE, or (multiple) virtual cards of various type	1	1	0	0	0	0	0	0	1	C1

4.3 Chip Type Coding

The Chip Type Coding indicates the chip type (high nibble) and memory size (low nibble), if available. Details see Table 9 and Table 10.

Note: For privacy protection the MIFARE Plus does not indicate the memory size in the default configuration.

Note: The current default configuration of the MIFARE DESFire or MIFARE DESFire EV1 does not include the Type Identification Coding in the ATS.

Table 9. Chip Type (high nibble)

Coding of Chip Type

	b7	b6	b5	b4	b3	b2	b1	b0	Hex
(Multiple) Virtual Cards (MIFARE or other)	0	0	0	0	x	x	x	x	0x
MIFARE DESFire	0	0	0	1	x	x	x	x	1x
MIFARE Plus	0	0	1	0	x	x	x	x	2x
RFU					x	x	x	x	3x…Fx

Table 10. Chip Type (low nibble)
Coding of Memory size

	b7	b6	b5	b4	b3	b2	b1	b0	Hex
<1 kByte	x	x	x	x	0	0	0	0	x0
1 kByte	x	x	x	x	0	0	0	1	x1
2 kByte	x	x	x	x	0	0	1	0	x2
4 kByte	x	x	x	x	0	0	1	1	x3
8 kByte	x	x	x	x	0	1	0	0	x4
RFU	x	x	x	x					x5…xE
Unspecified	x	x	x	x	1	1	1	1	xF

4.4 Chip Version Coding

The Chip Version Coding indicates the Status of the chip (low nibble) as well as the chip generation (high nibble), if available. Details see Table 11 and Table 12.

Note: The current default configuration of the MIFARE Plus Engineering samples does not include the Type Identification Coding in the ATS.

Table 11. Chip Version (high nibble)
Coding of chip status

	b7	b6	b5	b4	b3	b2	b1	b0	Hex
Engineering samples	0	0	0	0	x	x	x	x	0x
RFU	0	0	0	1	x	x	x	x	1x
Released	0	0	1	0	x	x	x	x	2x
RFU					x	x	x	x	3x…Fx

Table 12. Chip Version (low nibble)
Coding of chip generation

	b7	b6	b5	b4	b3	b2	b1	b0	Hex
Generation 1	x	x	x	x	0	0	0	0	x0
Generation 2	x	x	x	x	0	0	0	1	x1
Generation 3	x	x	x	x	0	0	1	0	x2
RFU	x	x	x	x					x5…xE
Unspecified	x	x	x	x	1	1	1	1	xF

4.5 Coding of the Specifics

In the Specifics the capability for the virtual card selection of the chip is coded in the low nibble (see Table 13), and chip or customer specific details can be coded in the high nibble.

Table 13. Specifics (high nibble)
Coding of chip virtual card selection capability

	b7	b6	b5	b4	b3	b2	b1	b0	Hex
Only VCSL supported[7]	x	x	x	x	0	x	x	0	
VCS, VCSL, and SVC supported[8]	x	x	x	x	0	x	x	1	
all SLs supported[9]	x	x	x	x	0	0	0	x	
SL3 only card[10]	x	x	x	x	0	0	1	x	
RFU	x	x	x	x					x4…xD
no VCS command supported[11]	x	x	x	x	1	1	1	0	xE
Unspecified	x	x	x	x	1	1	1	1	xF

4.6 Default Coding of MIFARE cards

The default coding of the MIFARE products (release status) is shown in Table 14.

Table 14. MIFARE default Type Identification Coding in the ATS
Table description (optional)

Chip	Hex	Nickname
MF 3 ICD40	n.a.	MIFARE DESFire
MF 3 ICD21	n.a.	MIFARE DESFire EV1 2K
MF 3 ICD41	n.a.	MIFARE DESFire EV1 4K
MF 3 ICD81	n.a.	MIFARE DESFire EV1 8K
MF1PLUS60	C1 05 2F 2F 01 BC D6	MIFARE Plus X 2K
MF1PLUS80	C1 05 2F 2F 01 BC D6	MIFARE Plus X 4K
MF1SPLUS60	C1 05 2F 2F 00 35 C7	MIFARE Plus S 2K
MF1SPLUS80	C1 05 2F 2F 00 35 C7	MIFARE Plus S 4K

7. Details of virtual card selection refer to the AN Virtual Card Selection.
8. Details of virtual card selection refer to the AN Virtual Card Selection.
9. A MIFARE Plus S does not support SL2.
10. An SL3 only card might be available in the future.
11. Details of virtual card selection refer to the AN Virtual Card Selection.

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